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BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			RUTTEN,	RUTTEN, JAMES D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)		
	10/002,060	CABOT ET AL.		
Office Action Summary	Examiner	Art Unit		
	J. Derek Rutten	2192		
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address		
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 66(a). In no event, however, may a reply be tim rill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).		
Status				
 1) ☐ Responsive to communication(s) filed on <u>01 Not</u> 2a) ☐ This action is FINAL. 2b) ☐ This 3) ☐ Since this application is in condition for allowant closed in accordance with the practice under E 	action is non-final. ace except for formal matters, pro			
Disposition of Claims				
4) ☐ Claim(s) 1-28 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-28 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or				
Application Papers				
9)☐ The specification is objected to by the Examiner 10)☒ The drawing(s) filed on 31 October 2001 is/are: Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction 11)☐ The oath or declaration is objected to by the Examiner	a) accepted or b) objected or b) objected drawing(s) be held in abeyance. See on is required if the drawing(s) is obj	e 37 CFR 1.85(a). lected to. See 37 CFR 1.121(d).		
Priority under 35 U.S.C. § 119				
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 				
Attachment(s)				
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:			

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/19/2005 has been entered. Claims 1, 6, 11, 16, 20, and 25 have been amended. Claims 1-28 remain pending in the application and have been fully considered by the examiner.

Response to Arguments

- 2. Applicant has primarily argued that the claims are not anticipated by the Rivin reference because it does not disclose data samples including a level of memory utilization. This argument is persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Applicant's "Background" description appearing on pages 1 and 2 of the originally filed specification.
- 3. Applicant's arguments regarding the objection to the drawings have been considered and are persuasive. Applicant's amendment to claim 25 has overcome the rejection under 35 U.S.C. § 112, second paragraph. Therefore, both the objection to the drawings and the rejection of claims 25 and 26 under 35 U.S.C. § 112, second paragraph have been withdrawn.

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4. Near the bottom of page 8 of the reply, Applicant argues that the cited references do not teach or disclose statistically distributed data samples. However, Rivin discloses a statistical profiling method for sampling data in a random manner (see column 2 lines 20-24). This would appear to meet the requirements for "statistically distributed" as described on page 3 line 12 of the originally filed specification. Therefore the argument is not convincing. Furthermore, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant has not explained why the data samples described in Rivin would not qualify as "statistically distributed".

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5. At the bottom of page 8, Applicant essentially argues that the Background section of the specification does not disclose a statistically distributed random inter-sample period. This argument is convincing. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of prior art of record U.S. Patent 6,718,286 to Rivin et al.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first and second data samples include a level of memory utilization" (claims 1, 11 and 20) must be shown or the feature canceled from the claims. No new matter should be entered.

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Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

- 7. The following is a quotation of the first paragraph of 35 U.S.C. 112:
 - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 8. Claims 1-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

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Independent claims 1, 11, and 20 call for "first and second data samples <that> include a level of memory utilization during program execution" (emphasis added). However, the description of the invention appearing on pages 3-11 of the originally filed specification does not provide a description of any data samples that include a level of memory utilization during program execution. The background of the invention, appearing on pages 1 and 2 of the specification, especially line 1 on page 2, describes utilization of a set of data samples to determine a "level of memory utilization of a computer processor while executing a simulation application". However, this description is provided in the context of the prior art, and does not explicitly and/or implicitly provide a description of how data samples include a level of memory utilization, as used in the claims. Moreover, is this "level" predetermined data/information? It is noted that in the amendment, the Applicant has not pointed out as to where amended limitations are supported by the originally filed disclosure to ensure that no new matter has been added. No further description could be found to indicate that the invention provides data samples that include a level of memory utilization. The dependent claims do not cure the

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9. The above rejection under 35 U.S.C. 112, first paragraph is related to new limitations regarding data samples that "include a level of memory utilization during program execution". For the purpose of further examination, this limitation will be interpreted in light of the "Background" section appearing on pages 1 and 2 of the originally filed specification, as data samples that are *used to determine* a level of memory utilization during program execution.

deficiencies of the base claims, and are rejected as being dependent upon rejected base claims.

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Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 11. Claims 1, 6, 7, 11, 16, 20, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art of record U.S. Patent 6,718,286 to Rivin et al. (hereinafter "Rivin") in view of Applicant's "Background" section appearing on pages 1 and 2 of the originally filed specification (hereinafter "the Background").

As per claim 1, Rivin discloses:

A method of sampling data (column 8 line 64 – column 10 line 10), comprising:
gathering a first data sample during execution of a program on a computing
device; executing the program during a random inter-sample period; and gathering a
second data sample following the inter-sample period ..., and wherein the first and
second data samples form at least a portion of a set of data samples, the set of data
samples to be used to determine a measure of performance of the computing device while
executing the program See column 2 lines 21-24:

The foregoing needs are addressed, and advantages obtained, by the use of a statistical profiling method which non-intrusively samples the processor's program counter in a random manner.

The technique of profiling with sampling inherently provides execution of a program between the gathering of samples, otherwise program data would not be available for profile analysis. Further, Rivin's technique of random sampling inherently requires a set of samples, since a variable inter-sample period between at least two samples is required for any sampling process to be called random.

Rivin does not expressly disclose wherein the first and second data samples are used to determine a level of memory utilization during program execution. However, in an analogous environment, the Background teaches that data samples can be used to determine a level of memory utilization. See page 1 line 21 – page 2 line 2:

The set of data samples is used to determine the performance of the instrument while performing the application, for example, the level of memory utilization of a computer processor while executing a simulation application. [emphasis added]

As per claim 6, the above rejection of claim 1 is incorporated. Rivin further discloses: wherein gathering the first data sample comprises: resetting data gathering hardware, executing the program during a sampling period; and stopping the data gathering hardware at the end of the sampling period, wherein data samples in the set of data samples are statistically distributed (see column 2 lines 20-24 and column 5 lines 36-46: Comment: Data gathering hardware is reset using the SAMPLE and DISABLE signals, the sample is collected, and the hardware is stopped through the removal of the signal).

As per claim 7, the above rejection of claim 1 is incorporated. Rivin further discloses: wherein gathering the first data sample comprises: starting data gathering hardware, executing the program during a sampling period; and stopping the data gathering hardware at the end of the sampling period (column 5 lines 36-46: Comment:

Data gathering hardware is started using the SAMPLE signal, the sample is collected, and the hardware is stopped through the removal of the signal).

As per claim 11, Rivin does not expressly disclose: An article comprising a machine-readable medium that stores machine-executable instructions for sampling data. However, in an analogous environment, the Background teaches use of a computer program product comprising a computer readable medium storing instructions for sampling data (page 1 lines 9-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the Background's computer program product with Rivin's sampling technique. One of ordinary skill would have been motivated to store executable code in program memory in order to execute the program. All further limitations have been addressed in the above rejection of claim 1.

As per claim 16, the above rejection of claim 11 is incorporated. All further limitations have been addressed in the above rejection of claim 6 and 7.

In regard to claim 20, Rivin discloses: An apparatus for sampling data, a memory that stores executable instructions; and a computer processor that executes the instructions (FIG. 1) ...

execute the application during a statistically distributed random inter-sample period. See column 2 lines 20-24:

The foregoing needs are addressed, and advantages obtained, by the use of a statistical profiling method which non-intrusively samples the processor's program counter in a random manner. [emphasis added]

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All further limitations have been addressed in the above rejection of claim 1.

In regard to claim 25, the above rejection of claim 20 is incorporated. All further limitations have been addressed in the above rejection of claim 6.

As per claim 26, the above rejection of claim 25 is incorporated. Rivin further discloses event count registers (Fig. 1 element 16).

12. Claims 2-5, 8, 12-15, 17, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivin and the Background as applied to claim 1 above, and further in view of prior art of record U.S. Patent 5,768,500 to Agrawal et al. (hereinafter referred to as "Agrawal").

As per claim 2, the above rejection of claim 1 is incorporated. Rivin does not expressly disclose: generating an inter-sample count; and decrementing the inter-sample count to zero before gathering the second data sample. However, in an analogous environment, Agrawal teaches the use of an event detector that triggers an interrupt for sampling when a count reaches a certain value (column 2 lines 37-41; also column 8 lines 26-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Agrawal's counter with Rivin's random sampling method. One of ordinary skill would have been motivated to implementing a systematic method for generating an interrupt to trigger a sample gathering event.

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As per claim 3, the above rejection of claim 2 is incorporated. Rivin further discloses: *performing overhead operations during the inter-sample period* (column 6 lines 54-60).

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As per claim 4, the above rejection of claim 3 is incorporated. Rivin further discloses: wherein the inter-sample count is longer than an execution time required to perform the overhead operations (column 4 lines 3-6 describes a sequential sampling which inherently requires that the sample is stored before another sample is collected.).

As per claim 5, the above rejection of claim 3 is incorporated. Rivin further discloses: wherein the overhead operations include at least one of decrementing the inter-sample count, storing a data sample, and performing a calculation based on a data sample (column 6 lines 54-60).

As per claim 8, the above rejection of claim 7 is incorporated. Rivin does not expressly disclose event counters. However, Agrawal teaches the use of event counter registers (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Agrawal's registers with Rivin's sampling method. One of ordinary skill would have been motivated to track the execution of a program and collect samples based on the frequency of interesting events.

As per claims 12-15, the above rejection of claim 11 is incorporated. All further limitations have been addressed in the above rejections of claims 2-5, respectively.

As per claim 17, the above rejection of claim 16 is incorporated. All further limitations have been addressed in the above rejection of claim 8.

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As per claim 21, the above rejection of claim 20 is incorporated. The background section does not expressly disclose: a decrementing register; generating an inter-sample count; and decrementing the inter-sample count to zero before gathering the second data sample. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Agrawal's counter with the sampling method of the background section. One of ordinary skill would have been motivated to implement a systematic method for generating an interrupt to trigger a sample gathering event. All further limitations have been addressed in the above rejection of claim 2.

13. Claims 9, 10, 18, 19, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Rivin, the Background, and Agrawal as applied to claim 2 above, and further in view of prior art of record U.S. Patent 3,700,869 to Low et al. (hereinafter "Low").

As per claim 9, the above rejection of claim 9 is incorporated. Rivin and Agrawal do not expressly disclose a linear feedback shift register. However, in an analogous environment, Low teaches that a linear feedback shift register can be used to produce a random bit pattern (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's teaching of a linear feedback shift register in Agrawal's counter with Rivin's sampling method. One of ordinary skill would have been motivated to use an efficient arrangement for generating a random binary sequence.

As per claim 10, the above rejection of claim 9 is incorporated. Rivin and Agrawal do not expressly disclose primitive trinomials. However, Low teaches a linear feedback shift register that is characterized by a primitive trinomial (column 1 lines 26-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's primitive trinomials corresponding to a linear feedback shift register in Agrawal's counter with Rivin's sampling method. One of ordinary skill would have been motivated to use a binary sequence corresponding to a primitive trinomial since it is a natural characteristic of using a two-tap linear feedback register which provides an efficient arrangement for generating a random binary sequence.

As per claims 18 and 19, the above rejection of claim 12 is incorporated. All further limitations have been addressed in the above rejections of claims 9 and 10, respectively.

As per claim 27, the above rejection of claim 21 is incorporated. Rivin further discloses shift registers (see column 2 lines 28-32). The Rivin does not expressly disclose: a linear feedback shift register, and wherein the computer processor executes an instruction to enable the linear feedback shift register to produce a bit pattern that corresponds the inter-sample count. However, in an analogous environment, Low teaches that a linear feedback shift register can be used to produce a random bit pattern (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's teaching of a linear feedback shift register bit patterns with Rivin's shift register. One of ordinary skill would have been motivated to use an

efficient arrangement for generating a random binary sequence (Low column 1 lines 21-25).

As per claim 28, the above rejection of claim 27 is incorporated. Rivin does not expressly disclose primitive trinomials. However, Low teaches a linear feedback shift register that is characterized by a primitive trinomial (column 1 lines 26-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's primitive trinomials corresponding to a linear feedback shift register with Rivin's shift register. One of ordinary skill would have been motivated to use a binary sequence corresponding to a primitive trinomial since it is a natural characteristic of using a two-tap linear feedback register which provides an efficient arrangement for generating a random binary sequence.

14. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Riven, the Background, and Agrawal as applied to claim 22 above, and further in view of prior art of record "Interrupts", Daqarta, DMA, and FIFO, 2001, appearing on the Information Disclosure Statement by Applicant as designation "AR" dated March 31, 2003 (hereinafter "Daqarta").

As per claim 22, the above rejection of claim 21 is incorporated. The background section discloses overhead operations (page 2 lines 6-12). The background section further discloses running an application during the inter-sample period (page 1 lines 17-20). The background section does not expressly disclose overhead operations *during the inter-*

sample period. However, in an analogous environment, Daqarta teaches that overhead operations are performed during an inter-sample period (page 2 paragraph 1 describes a DMA controller that performs overhead operations including sample storage while the CPU continues execution). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Daqarta's teaching of overhead processing with the background section's. One of ordinary skill would have been motivated to store one sample while an application or CPU is running in order to use a minimum amount of time (Daqarta page 2 paragraph 1).

As per claim 23, the above rejection of claim 22 is incorporated. The background section further discloses increasing the time between samples (page 2 lines 13-15; Comment: This inherently requires an inter-sample time longer than overhead execution, since if it was not, then the entire time would be spent on overhead, and no program execution could be accomplished).

As per claim 24, the above rejection of claim 22 is incorporated. The background section further discloses: perform overhead operations that include instructions for at least one of decrementing the inter-sample count, storing a data sample, and perform a calculation based on a data sample (page 2 lines 6-12).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,158,024 to Mandal discloses using data samples to determine a level of memory utilization (See column 2 lines 55-64).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571) 272-3703. The examiner can normally be reached on T-F 6:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jdr

TUAN DAM SUPERVISORY PATENT EXAMINER